UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/682,323	10/09/2003	Joseph A. Yedinak	90065.000431/17732.56390.	9818

7590 05/04/2006

Laurence S. Roach, Esq.
Law Office of Thomas R. FitzGerald
Suite 210
16 E. Main Street
Rochester, NY 14614-1803

EXAMINER	
DICKEY, THOMAS L	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	**Application No.** 10/682,323	**Applicant(s)** YEDINAK ET AL.
	Examiner Thomas L. Dickey	**Art Unit** 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20,21,24,25 and 39* is/are rejected.

7)☒ Claim(s) *22,23,26-38 and 40-44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/21/06 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 41 and 42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. In claim 41, line 14, "said integrated circuit" has no antecedent basis.

B. In claim 42, line 17, "said die street" has no antecedent basis; and in line 18, "said integrated circuit" has no antecedent basis.

Correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 20,21,24,25, and 39 stand rejected under 35 U.S.C. 102(b) as being anticipated by NODA et al. (2001/0004124).

A. With regard to claims 20 and 21 Noda et al. discloses a power semiconductor device 10 with a substrate 2 having an active region (the active region is the central region shown generally below central plate 15-4 in figure 6) disposed in the central region of the substrate 2 and defined by first 6 and second 24 regions highly doped with opposite polarities (6: n-type, 24: p-type) of dopant; and an outer edge (the edge of substrate 2 is marked by part 3); an insulating layer 8 over the substrate 2 and between the active region and the edge of the substrate 2; at least three field plates 11A (although figure 6 shows only one field plate 11A the specification makes clear that the number of plate electrodes is not so limited. Noda et al. state, "If necessary, three, four or more plate electrodes may be provided." Note paragraph 0101) on the insulating layer 8 and disposed between the active area and the outer edge of the substrate 2, said field plates 11A each having an outer edge facing the edge of the substrate 2 and an inner edge facing the active region; and means (a capacitive voltage divider network Ca_1, Ca_2, Cb_1, C_{b2}, etc) for generating voltage potentials applied to the field plates 11A such that each field plate 11A has an applied voltage potential such that the voltage potential difference between the first and second field plates 11A is different from the voltage potential difference between the second and third field plates 11A to generate electric fields in the substrate 2 below the field plates 11A wherein said electric fields have substantially the same contours. Note figure 6 and paragraphs 0080-0091 and 0097-0102 of Noda et al.

B. With regard to claims 24 and 25 Noda et al. discloses a power semiconductor device 10 with a substrate 2 having an active region (the active region is the central region shown generally below central plate 15-4 in figure 6) disposed in the central region of the substrate 2 and defined by first 6 and second 24 regions highly doped with opposite polarities (6: n-type, 24: p-type) of dopant; and an outer edge (the edge of substrate 2 is marked by part 3); an insulating layer 8 over the substrate 2 and between the active region and the edge of the substrate 2; at least three field plates 11A (although figure 6 shows only one field plate 11A the specification makes clear that the number of plate electrodes is not so limited. Noda et al. state, "If necessary, three, four or more plate electrodes may be provided." Note paragraph 0101) on the insulating layer 8 and disposed between the active area and the outer edge of the substrate 2, said field plates 11A each having an outer edge facing the edge of the substrate 2 and in inner edge facing the active region; means (a capacitive voltage divider network Ca_1, Ca_2, Cb_1, C_{b2}, etc) for applying different voltage bias levels to each field plate 11A wherein the applied different voltage bias level generates electric fields in the substrate 2 below the field plates 11A and wherein said electric fields below said field plates 11A have contours varying from the outer edge of the each field plate 11A to the inner edge of each field plate 11A, wherein the contours of each electric field in the substrate 2 in the regions below each field plate 11A is substantially the same, so that the contours of each electric field below two or more field plates 11A are substantially the same. Note figure 6 and paragraphs 0080-0091 and 0097-0102 of Noda et al.

C. With regard to claim 39 Noda et al. discloses a method of controlling the electric field concentration on the outside edge of a power semiconductor device comprising, in a substrate 2 having a central region (the central region is shown generally below central plate 15-4 in figure 6) and an edge (the edge of substrate 2 is marked by part 3), forming an active region (the active region is the central region shown generally below central plate 15-4 in figure 6) of a power semiconductor device comprising first 6 and second 24 regions highly doped with opposite polarities (6: n-type, 24: p-type) of dopant; forming an insulating layer 8 between the active region and the edge; disposing a plurality of field plates 11A (although figure 6 shows only one field plate 11A the specification makes clear that the number of plate electrodes is not so limited. Noda et al. state, "If necessary, three, four or more plate electrodes may be provided." Note paragraph 0101) on said die, said field plates 11A being spaced apart relative to each other; dividing (by the use of capacitive voltage divider network Ca_1, Ca_2, Cb_1, C_{b2}, etc) a potential difference to generate a different bias voltage for each field plate 11A; and applying the respective different potentials to the respective field plates 11A to generate electric fields in the substrate 2 that have substantially the same electric field contours. Note figure 6 and paragraphs 0080-0091 and 0097-0102 of Noda et al.

Allowable Subject Matter

4. Claims 22 and 23 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a power semiconductor device having every limitation of claim 20 (as said claim 20 is today rejected over Noda et al.), and in addition a means for generating voltage potentials comprising a voltage divider network of resistors, as recited in claim 22.

5. Claims 26-38 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a power semiconductor device having every limitation of claim 24 (as said claim 24 is today rejected over Noda et al.), and in addition a means for applying different voltage bias levels comprising a voltage divider network including a plurality of resistive elements connected in series to each other for generating said different bias voltages, each of said bias voltages being dependent at least in part upon a corresponding one of said resistive elements as recited in claim 26.

6. Claims 40, 43, and 44 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a method of controlling electric field concentration having every limitation of claim 39 (as said claim 39 is today rejected over Noda et al.), and in addition that said dividing step comprises electrically connecting one or more polysilicon resistors between said edge and one of an emitter and gate of said power semiconductor device, as recited in claim 40, or in addition that said disposing step comprises disposing first, second and third field plates on said die, said first field plate being relatively proximate to said die edge, said second field plate being disposed between said first and second field plates, and said third field plate being disposed relatively distant from said die street and proximate the active region; and said applying step comprises applying a first, second and third bias voltage to said first second and third field plates, respectively, said first bias voltage having a value of from approximately fifty to approximately sixty percent of said potential difference, said second bias voltage having a value of from approximately twenty to approximately thirty percent of said potential difference, and said third bias voltage having a value of from approximately fifteen to approximately twenty percent of said potential difference, as recited in claim 43.

Response to Arguments

7. Applicant's arguments filed 04/21/06 have been fully considered but they are not persuasive.

It is argued, at page 10 of the remarks, that "The Examiner states that the active area is generally below the metal electrode 15-4 (Fig. 6)." However, the Examiner lacks the power to define the scope of any claim term. See Salazar v. Procter & Gamble Co., 75 USPQ2d 1369 (CA FC 2005) ("[A]s previously discussed, this court finds that the examiner's unilateral remarks did not alter the scope of the claim").

It is argued, at page 10 of the remarks, that "([Noda et al.'s] field plates 11A and 12A are disposed underneath the metal electrodes (Fig. 6). Thus, field plates are within the active region." Here applicant appears to have stretched the truth about what Noda et al. discloses in order to make a point. In fact only Noda et al.'s plate 12A (Noda et al.'s device has only one plate 12A) is disposed underneath metal electrode 15-4. Noda et al.'s filed plates 11A (one is shown, many are present. Note paragraph 0101) are not located under metal electrode 15-4. Applicant should note that the Examiner never asserted that the single plate 12A met any claim term. The Examiner asserts that multiple plates 11A meet the claim term "a plurality of field plates dispos[ed] on said die [and] spaced apart relative to each other."

It is argued, at page 10 of the remarks that "The field plates of the invention are outside of the active region of the claimed device See Figure 4A of the application. Note how the emitter (source) 50 is to the right and edge of the die is to the left." There is no part 50 in figure 4A. In referring to part 50 Applicant apparently meant to refer to the part marked "EMMITER (sic) METAL." It is noted, however, that the active area of the claimed device is required to comprise two highly doped regions. Claim 20 lines 3 and 4. Figure 4A does not show two highly doped regions to the right of field plates 42 and 44.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas L. Dickey
Patent Examiner
Art Unit 2826
12/05